DESIGN OF LOW POWER NOVEL GATE

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Abstract: Reversible logic gate design recovers the output from the input itself which is the novel gate for low power. This technology is widely used in VLSI design due to its low power. To achieve this, the number of input and outputs in the gate is equal. The function of the logic gates purely depends on the quantum cost function. Garbage output of the gates is ignored. Varieties of logic gates are available in the VLSI design. In this paper, different reversible logic gate functions are discussed. Also, it compares different adders with different gates.

Keywords: Quantum Cost, Garbage Output, Low Power, VLSI.

I. INTRODUCTION

Area delay product parameter is one of the main concerns in VLSI design as it decides whether the circuit is best or not. Power consumption is one of the major issues in any type of VLSI circuit. Because of every interconnection, the power will dissipate and finally major loss the power in the output side. Most of the digital logic circuits are easy and complex in nature. The novel reversible logic design allows the subsystem logic circuit with low power dissipation approximately zero power dissipation. The breakdown of power in the circuits relates with ever-increasing the attractiveness of portable electronic devices. All battery using components like Laptop, pagers, portable video players and cellular phones are the major source of power.

II. RELATED WORKS

An ALU design with the concept of reversible computing is discussed in [1]. Reversible logic gates are replaced by the conventional gates. It performs the same operation as conventional ALU design. The design of efficient adder circuits is based on the Howser North Gate (HNG) and Prese gates. HNG and Prese full adder gates are used to design the lower hardware complexity and low power adder circuit.

Carry look ahead adder design by using Multi Input Floating Gate (MIFG) is described in [2]. Mobile gadgets have mixed mode circuits which require low power and low voltage. These circuits are embedded with analog sub-sections.4-bit full adder is designed using the reconfigurable logic of MIFG MOSFETs. It requires only 1.8V for its operation.

The analysis of a low power CMOS full adder is illustrated in [3]. It consists of three modules and each module has its own design. All are simulated, analyzed, and then compared. A full adder cell with CMOS output drive is discussed in [4] that uses a hybrid pass logic. XNOR and XOR gates are generated using this logic ver effectively. Also, a CMOS style is designed with a good drivability carry out and regular structure. It is shown that a better power-delay efficient is achieved above 2.4V ranges Thus, it is suitable for embedded applications which require high performance ALU and low power.

The construction of a quantum-mechanical Hamiltonian describing a computer is given in [5]. Based on a sequence of logic steps, a dynamical evolution is generated by Hamiltonian if all logical steps are locally reversible. The presence of noise produces computational errors which can be corrected by redundancy.

Reversible rationale doors are particularly popular for the future figuring advancements as they are known to deliver zero power dispersal under perfect conditions [6]. An enhanced plan of a multiplier utilizing reversible rationale entryways is discussed. Multipliers are extremely basic for the development of different computational units of a quantum PC.

The reversible logic gates for efficient utilizations are described in [7]. The reversible logic is used to improve the power utilizations as well as the computational delay reductions. There are various reversible gates are mainly used that is Fredkin gate and peres gate.

An implementation of the digital circuits based on the reversible logical gates is discussed in [8]. The main purpose of the reversible logic gate is to reduce the number of logical elements utilizations. By using the reversible gate, the digital circuit is implemented with the efficient power consumptions.

Reversible logic gates based circuits design for the requirement of low power circuits is described in [9]. In a conventional combinatorial logic gates, the loss of information can not be recovered as it dissipates heat. The heat is produced due to the loss of information during operation. To overcome this, reversible logic gates are used for the construction which allow the recovery of the information.

II. REVERSIBLE LOGIC GATES

It is the most successful design for computer as it generates less amount of heat inside the computer. Energy efficiency in the circuit can be achieved by reversible logic computing architecture. Normally energy efficiency is achieved by changing the speed of circuits and by reducing the delay such as micro and nano-electronic. To enhance the portability of devices, the circuits are designed by reversible logic circuit. The component size of the circuit decreases the overall size of the device and thus the outcomes are portable. Figure 1 shows the basic reversible logic circuit.

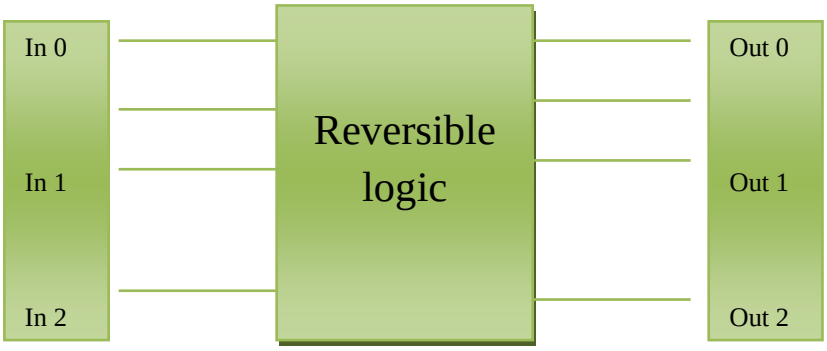

Fig. 1 Basic Reversible Logic Circuit

A. Feynman Gate

Figure 2 shows the Feynman gate which is also referred as controlled NOT gate. It consists of two inputs and two outputs. Figure 2 shows the Feynman gate operation clearly. The quantum cost of Feynman gate is one.

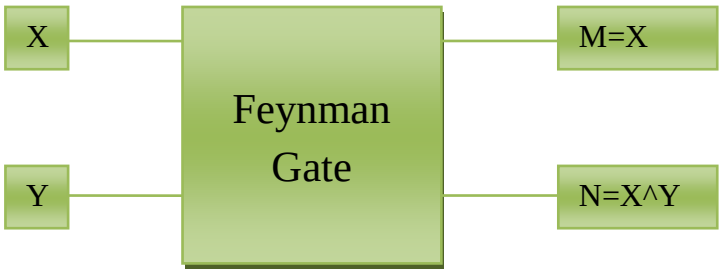

Fig. 2 Block of Feynman Gate

B. Fredkin Gate

Fredkin gate is also referred as controlled permutation gate. It contains three inputs and three equal outputs. The basic gate function is shown in Figure 3.

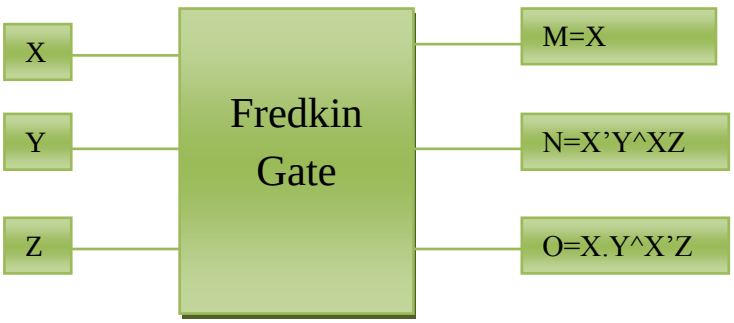

Fig. 3 Fredkin Gate

C. Peres Gate (PG)

It is also referred as new Toffoli gate. It has three inputs and three output gates. It is also constructed by using 1 Toffoli and 1 Feynman gate. Figure 4 shows the Peres gate. The quantum cost of the PG is four.

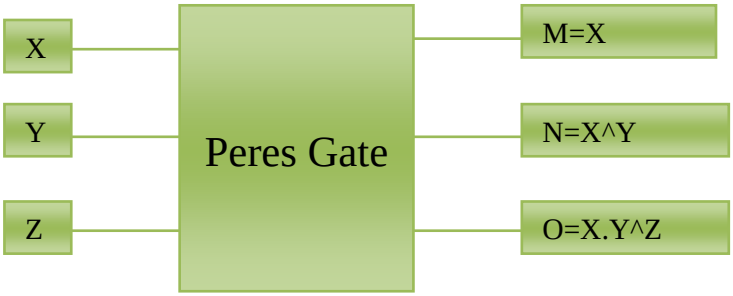

Fig. 4 Peres Gate

Figure 5 shows the full adder circuit which is constructed by using two PGs. The two PGs are cascaded to each other. The output of the first stage is forwarded to the second PG as inputs. It reduces the power consumption compared to the normal full adder circuit.

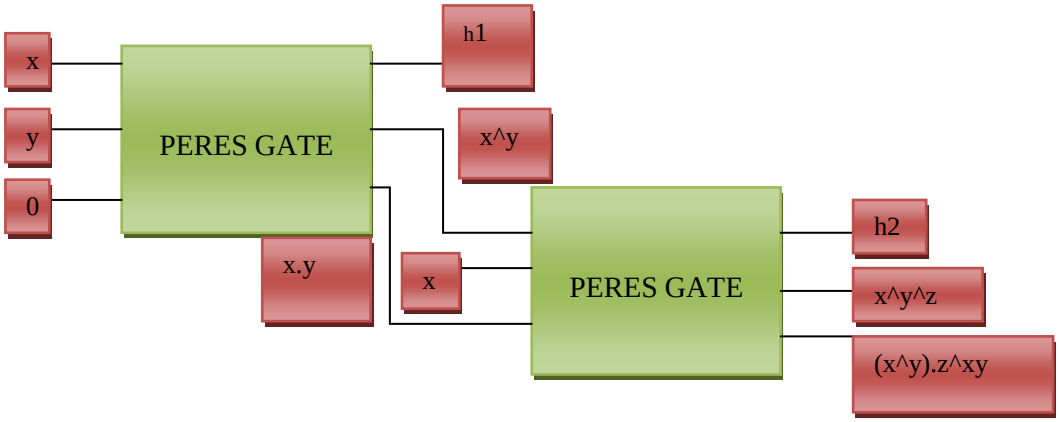

Fig. 5 Full Adder using Peres Gate

V. RESULTS AND DISCUSSION

The adder circuit can be synthesized and evaluated using Xilinx simulation environment, and also compared with the traditional full adder circuit. Table 1 shows the quantum cost, garbage output, and delay of two full adder circuit using PG and HNG gates.

TABLE 1 Comparison of Adder circuits

Parameters	Adder using Peres Gate	Adder using HNG
Quantum Cost	126	98
Garbage Output	30	32
Delay (ns)	7.74	7.78

VI. CONCLUSION

In this paper, reversible logic gates using different adder circuits were designed and compared with some parameters to known the best adders. Delay and quantum cost should be reduced for proposed adder circuit. The proposed reversible loge gate provides better power optimization when compared to the irreversible logic gate. It reduces 22% of quantum cost and 10% of garbage cost. Also, it reduces 5% of delay.

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